REMARKS

Claims 1-85 are currently pending, of which claims 12-61, 69-73 and 81-85 have been allowed. Applicant reserves the right to pursue original and other claims in this and any other application. Applicant appreciates the indication of claims 12-61, 69-73, and 81-85 being allowed.

Claims 1-8, 62-65, and 74-77 stand rejected under 35 U.S.C. 102(e) as being anticipated by Chen Hsu et al. (U.S. Pat. No.6483,764)("Chen"). The rejection is respectfully traversed.

Claim 1 recites a memory refresh circuit comprising "a control circuit for conducting a memory refresh operation, for monitoring a memory device, and for indicating when said refresh operation is complete based on said monitoring of said memory device."

Chen discloses:

> A novel DRAM refresh method and system and a novel method of designing a low-power leakage monitoring device. With the DRAM refresh method, the time is adjusted based directly on the cell leakage condition. The method of designing a low-power leakage monitoring devices uses a memory cell identical to the cells in the real array. This monitor cell is designed so that it will represent the average cell or the worst cell leakage condition. If the leakage is severe, the refresh cycle time is significantly reduced, or halved. If the leakage level is very low or undetectable, then the refresh cycle time is significantly increased, or doubled. If the leakage is moderate, or in the normal range, the refresh time is optimized, so that the power consumption used for DRAM refresh is minimized

(Chen Abstract)

Applicant respectfully submits that Chen fails to disclose at least a control circuit "for indicating when said refresh operation is complete based on said monitoring of said memory device." Chen is directed to determining when to schedule refresh operations based on memory cell power leakage, not when a "refresh operation is complete" which is an entirely different issue. As

noted above in Chen, if the leakage is severe, the time between refresh operations is decreased. If leakage is not severe, then time between refresh operations is increased. At no point is Chen determining when a "refresh operation is complete."

Applicant notes that the Office refers to elements 900, 910 and 920 of Chen's FIGs. 11, 12, 13, and 14 as support for Chen allegedly rendering the claimed invention unpatentable. Applicant, however, takes this opportunity to point out that elements 900, 910, 920 are not described in Chen's specification. Further, Applicant notes that Chen's description of FIGs. 11, 12, 13, and 14 is directed towards setting and adjusting time between refresh operations (i.e., refresh cycle time). According to Chen:

> FIG. 10 shows how the leakage monitor scheme may be implemented in a stand alone DRAM chip. In this embodiment, only one monitoring device and one refresh circuit component are included. A BIST engine 930 communicates with the leakage monitor and the self-refresh components. The refresh cycle time is adjusted based on the cell leakage condition. If the cell leaks more, it refreshes more frequently so the data integrity is maintained. If the cell leaks less, then the refresh rate becomes less frequent to minimize the power consumption.
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> With reference to FIG. 11, for a large DRAM, for example 1G and greater, commonly, a mult[i]-bank architecture is used. Here, in this embodiment of FIG. 11, each bank can have its own leakage monitor device and separated self-refresh components. With this arrangement, each bank may refresh with its own rate depending on the cell leakage condition of that bank.
>
> FIG. 12 illustrates an embedded DRAM cache. One or more leakage monitor devices and self-refresh circuit components can be included. A BIST refresh rate of each individual DRAM array.
>
> FIG. 13 shows several DRAM chips installed in a module. Each chip may have its own leakage monitoring device and refresh circuits. A BIST engine inside a CPU chip will issue a monitor signal to each chip to evaluate the leakage level of each chip and to adjust the refresh cycle for each chip.
>
> FIG. 14 shows a flow char of the intelligent refresh. The operating sequence is described below. (1) A BIST engine 1315 issues a refresh command to pre-charge the monitor cell 1320 and to activate the self-

> refresh circuit 1310. (2) The self-refresh circuit 1310 starts the refresh operation from the first word-line address 1330. (3) After refreshing the last word-line address 1350, the monitor cell is evaluated 1360. (4) The monitor cell will be recharged after evaluation is done 1370. (5) The result of evaluation will be used to adjust the refresh cycle time through a control circuit 1390. (6) The new refresh cycle time will be used in the following refresh cycle from the first word-line to the last word-line, and so on.

(Chen, Col. 6, line 46 – Col. 7, line 20) Thus, Chen fails to anticipate the claimed invention and the rejection of claim1 and its dependant claims should be withdrawn and the claims allowed.

Claims 62 and 74 also recite a circuit "for indicating when said refresh operation is complete based on said monitoring of said memory array." Thus, claims 62 and 74 and their respective dependant claims are allowable over Chen for at least the reasons noted above with respect to claim 1. The rejection should be withdrawn and the claims allowed.

Claims 1-8, 62-65, and 74-77 stand rejected under 35 U.S.C. 102(e) as being anticipated by Miyamoto et al. (U.S. Pat. No.6,654,303)("Miyamoto"). The rejection is respectfully traversed.

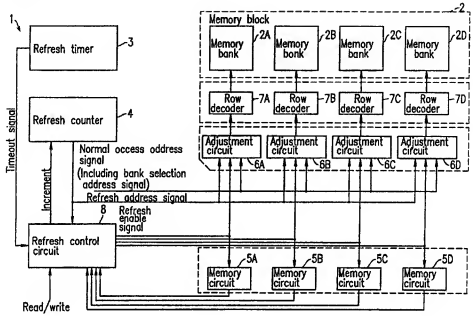
Claim 1 recites a memory refresh circuit comprising "a control circuit for conducting a memory refresh operation, for monitoring a memory device, and for indicating when said refresh operation is complete based on said monitoring of said memory device."

Miyamoto discloses a method of controlling refreshing operations in a memory device. Miyamoto's device includes a refresh control circuit 8, which is depicted in Miyamoto's FIG. 1 (reproduced below). According to Miyamoto:

> The refresh control circuit 8 controls the refresh operation according to the present invention and determines, in response to a read/write signal input from an external device or the timeout signal from the refresh timer 3, whether or not the refresh operation is required to be performed on any one of the memory banks 2A-2D based on refresh information stored in a corresponding one of the memory circuits 6A-6D so as to create a refresh enable signal.

(Miyamoto, Col. 6, lines 48-55)

FIG. 1



Miyamoto, FIG. 1

Miyamoto fails to disclose or suggest a control circuit "for monitoring a memory device, and for indicating when said refresh operation is complete based on said monitoring of said memory device." The Office mistakenly relies on Miyamoto Col. 6, lines 48-65 to support the argument that the Miyamoto's monitoring is the same as the claimed invention. At best, Miyamoto relies on a clock signal, and more specifically, a timeout signal to indicate when a memory refresh operation should be done (not when it is completed). Contrary to the suggestion of the Office, Miyamoto does not monitor a memory for determining when a refresh operation is complete; Miyamoto by contrast monitors a refresh timer 3 that establishes a time period in which the completion of a refresh operation should occur. Miyamoto discloses that refresh timer 3:

> measures a period of time for a refresh operation to be completed at a designated address, i.e., a critical amount of time for a memory cell to hold data, and outputs the timeout signal to the refresh control circuit

> 8 when the period of time for a refresh operation to be completed lapses.

(Miyamoto, Col. 4, lines 17-21) Thus, Miyamoto does not "monitor…a memory device" and "indicat[e] when said refresh operation is complete based on said monitoring of said memory device." The Office impermissibly and without any reasonable basis interprets that "the refresh timer measures a period of time for a refresh operation to be completed is considered to be the monitoring of memory device 1 in the corresponding refresh operation." (Office Action, p. 5)

As noted by the Office, Miyamoto's device monitors timer device 3 and not the memory to determine when a refresh operation is complete. Therefore, at best and as indicated by the Office, Miyamoto "measures a period of time for a refresh operation to be completed." (Office Action, page 2) Applicant notes that a refresh operation can take a shorter or longer amount of time than the time period that was pre-allocated by the timer 3. Miyamoto's FIGs. 2-4 reflect the invention of Miyamoto as being reliant on timing signals. FIGs. 2-4 are timing charts showing the operation of Miyamoto and explaining refresh operations when the timeout signal is output. Miyamoto's reliance and measurement of time periods is different from, and is not analogous to, the claimed invention's "monitoring a memory device," As such, Miyamoto fails to disclose "monitoring a memory device" and "indicating when said refresh operation is complete based on said monitoring of said memory device." Therefore, Miyamoto is different from the claimed invention and fails to anticipate the claimed invention for at least that reason. Therefore, the rejection of claim 1 should be withdrawn and the claim allowed.

Claims 2-8 depend from claim 1 and are allowable for at least the reason noted above with respect to claim 1.

Claims 62 and 74 recite similar limitations as claim 1 and are allowable for at least the reasons noted above with respect to claim 1.

Claims 63-65 and 75-77 depend from claim 62 and 74, respectively, and are allowable for at least the reason noted above with respect to claim 1.

Claims 9-11, 66-68, and 78-80 stand objected to as being dependant upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully submits that the base claims are allowable for at least the reasons set forth above. Thus, claims 9-11, 66-68, and 78-80 are allowable. The objection should be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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